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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,884	07/12/2001	Ronald J. Melanson	03226/053002;P5039	3596

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EXAMINER	
CHASE, SHELLY A	
ART UNIT	**PAPER NUMBER**
2133	8

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/904,884	MELANSON ET AL.
	Examiner	Art Unit
	Shelly A Chase	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 16 are presented for examination.

Response to Amendment

2. The rejection of claims 1 to 4, 6 to 10 and 12 to 16 under 35 USC as being anticipated by Lordi is **maintained**.

3. The rejection of claims 5 and 11 as being obvious over Lordi in view of Plants is **maintained**.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1 to 4, 6 to 10 and 12 to 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lordi.

Claim **1**:

Lordi substantially discloses a memory unit being corrected via error detection and error correction through a micro-controller (see fig. 2), the system comprising; a static random access memory (SRAM 1) and a second memory (SRAM2) (see col. 2, lines 40 to 45), and a parity selection logic [50] for receiving data from SRAM1 and SRAM2 (see col. 2, lines 50 to 52). Lordi also teaches that a multiplexer [40] is connected to SRAM1 and SRAM2 via data lines [32 & 34] and the mulitplexer selects

data from SRAM2 if the parity select logic detects an error in the read data (see col. 2, lines 65 et seq.), which reads on "wherein input selection of the multiplexer is controlled by an output of the error checking circuit."

Lordi does not specifically teach the error checking circuit is electrically disposed between the first memory bank and the multiplexer; however, Lordi teaches a parity checker connected between a controller and a multiplexer checking the data read form either a first or second memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the parity checker of Lordi by switching its connection to achieve the claimed connection, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to change the location of the parity checker in order to minimize processing time while using existing hardware as taught by Lordi (see col. 1, lines 20 to 25).

As per claims **2** and **3**, Lordi teaches the memories are SRAM (see col. 2, lines 33 to 35) and a parity checking device for detecting errors (see col. 2, lines 50 to 51).

As per claim **4**, Lordi discloses the parity select logic selects data from the primary memory if no errors are found and select data from the backup memory if an error is detected on the data read (see col. 2, lines 60 et seq.).

As per claim **6**, Lordi discloses simultaneous read and write operations for the memory devices (see col. 4, lines 1 to 12).

Claims **7** and **16**:

Lordi substantially discloses a memory unit being corrected via error detection and error correction through a micro-controller (see fig. 2), comprising; a static random access memory (SRAM 1) and a second memory (SRAM2) (see col. 2, lines 40 to 45), and a parity selection logic [50] ("means for error checking") for receiving data from SRAM1 and SRAM2 and parity checking the data for errors outputting a signal to select data from either the primary memory or the backup memory(see col. 2, lines 50 to 52). Lordi also teaches a simultaneous read and write process to the memories (see col. 4, lines 18 to 11), and that a multiplexer [40] is connected to SRAM1 and SRAM2 via data lines [32 & 34] wherein the mulitplexer selects data from SRAM2 if the parity select logic detects an error in the read data (see col. 2, lines 65 et seq.).

Lordi does not specifically teach the error checking circuit is electrically disposed between the first memory bank and the multiplexer; however, Lordi teaches a parity checker connected between a controller and a multiplexer checking the data read form either a first or second memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the parity checker of Lordi by switching its connection to achieve the claimed connection, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to change the location of the parity checker in order to minimize processing time while using existing hardware as taught by Lordi (see col. 1, lines 20 to 25).

As per claims **8** to **10**, Lordi discloses the memory devices are static random access memories (SRAM1 and SRAM2), a parity select logic [50] detecting and correcting errors and a multiplexer for selecting data from the primary memory or the backup memory.

Claim **12**:

Lordi substantially discloses a method for error correction and detection for a memory unit, the method comprising: a simultaneous read and write operation to (SARM1 and SARM 2), (see col. 4, lines 1 to 13), a RAM select logic selects the address for data to be read from the first or second SRAM (see col. 3, lines 35 to 42), and a parity select logic [50] checking the data read from specified locations of both SRAm1 and SRAM2 for errors and outputting a signal to select data based on the detection of errors (see col. 2, lines 40 et seq.).

Lordi does not specifically teach the error checking circuit is electrically disposed between the first memory bank and the multiplexer; however, Lordi teaches a parity checker connected between a controller and a multiplexer checking the data read form either a first or second memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the parity checker of Lordi by switching its connection to achieve the claimed connection, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to change the location of the parity

checker in order to minimize processing time while using existing hardware as taught by Lordi (see col. 1, lines 20 to 25).

As per claims **13** to **15**, Lordi discloses parity selects logic for detecting errors, a multiplexer [40] selecting data and data and parity stored in the memory are read by a byte (see fig. 5).

6. Claims **5** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lordi in view of Plants.

As per claims **5** and **11**, Lordi does not clearly teach that the first and second memory, the error checking means and the selection means are implemented on a single chip. However, Plants in an analogous art teaches a method for error checking in the configuration SRAM of a field programmable array (FPGA) wherein the configuration SRAM, a user SRAM a CRC circuit and a multiplexor are implemented in a FPGA (see col. 4, lines 15 to 25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify checking errors in the memory unit of Lordi to include all the elements on a single chip as taught by Plants since, Plants discloses utilizing a single chip aids in better performance and flexibility. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a method to achieve better performance when checking a memory unit for errors.

Response to Arguments

7. Applicant's arguments filed 2-9-2004 have been fully considered but they are not persuasive.

In response to the arguments concerning the previously rejected claims the following comments are made:

As to the argument on page 9, that Lordi error checking circuit does not check the data read from the first memory or the second memory for errors, the examiner disagrees with applicant's representative. Lordi teaches that the parity select logic determines if the data read is from the primary or backup memory and generates a select signal and the data is selected if there are no errors (see col. 3, lines 55 to 60). Therefore, Lordi substantially teaches the scope of the invention. I.e., Lordi teaches a method and an apparatus for reducing errors in a memory read employing a parity check logic and a multiplexer.

As to the argument on page 9, that the error checking circuit of Lordi cannot be, electrically disposed between either memory banks and the multiplexer as claimed, the examiner agrees with applicants representative that the error checking circuit of Lordi is not electrically connected as claimed; however the location of the parity checker as taught by Lordi substantially performs the function as claimed. Therefore, the location of the parity checker does not change the scope or purpose of checking the data read from either memory bank for errors.

As to the argument on page 11, that Plants fail to disclose the electrical connections of the error checking device, the examiner agrees with Applicants

representative; however, Lordi adequately supports the claimed limitation and the combination as a whole substantially teaches the claimed invention.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shelly A Chase

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